CLAIM AMENDMENTS

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided. The status of each claim is indicated in the parenthetical expression adjacent to the corresponding claim number.

Claims 1 - 27 (**Canceled**).

28. (**Currently Amended**): A semiconductor memory cell including at least one transistor to constitute the memory cell, the at least one transistor of the memory cell comprising:

a source region;

a drain region;

a body region disposed between the source region and the drain region, wherein the body region is electrically floating; and

a gate disposed over the body region; and

wherein the memory cell includes:

a first data state representative of a first charge in the body region; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region.

29. (**Previously Presented**): The memory cell of claim 28 wherein the first charge is comprised of an accumulation of majority carriers in the body region.

30. **(Previously Presented)**: The memory cell of claim 29 wherein the body region is comprised of a P-type semiconductor material and the source and drain regions are comprised of an N-type semiconductor material.

31. **(Previously Presented)**: The memory cell of claim 29 wherein the majority carriers accumulate in a portion of the body region that is adjacent to the source region.

32. **(Previously Presented)**: The memory cell of claim 28 wherein positive voltages are applied to the drain region and the gate to provide the second charge in the body region.

33. **(Previously Presented)**: The memory cell of claim 28 wherein positive voltages are applied to the drain region and the gate to remove at least the first charge from the body region.

34. **(Previously Presented)**: The memory cell of claim 33 wherein, in response to positive voltages being applied to the drain region and the gate, the transistor of the memory cell includes a junction between the body region and the source region, wherein the junction is forwarded biased.

35. **(Previously Presented)**: The memory cell of claim 33 wherein, in response to the positive voltages being applied to the drain region and the gate, the transistor of

the memory cell includes a forward bias current between the body region and the source region.

36. **(Previously Presented)**: The memory cell of claim 33 wherein the second charge is stored in the body region in response to removing the positive voltages from the drain region and the gate.

37. **(Currently Amended)**: A semiconductor memory cell including at least one transistor to constitute the memory cell, the at least one transistor of the memory cell comprising:

a source region having impurities to provide a first conductivity type;

a drain region having impurities to provide the first conductivity type;

a body region disposed between the source region and the drain region wherein the body region is electrically floating and includes impurities to provide a second conductivity type wherein the second conductivity type is different from the first conductivity type;

a gate disposed over the body region;

wherein the memory cell includes:

a first data state representative of a first charge in the body region wherein the first charge is substantially provided by impact ionization; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region.

38. **(Previously Presented)**: The memory cell of claim 37 wherein the first charge is comprised of majority carriers and wherein the second conductivity type is a P-type.

39. **(Previously Presented)**: The memory cell of claim 37 wherein, in response to a first positive voltage applied to the drain region and a second positive voltage applied to the gate, at least the first charge is removed from the body region through the source region.

40. **(Previously Presented)**: The memory cell of claim 39 wherein the memory cell, in response to the first and second positive voltages, includes a junction between the body region and the source region which is forwarded biased.

41. **(Previously Presented)**: The memory cell of claim 40 wherein the first conductivity type is an N-type.

42. **(Previously Presented)**: The memory cell of claim 41 wherein the second charge is stored in the body region in response to removing the first positive voltage from the drain region before removing the second positive voltage from the gate.

43. **(Previously Presented)**: The memory cell of claim 41 wherein, in response to the first and second positive voltages, the transistor includes a forward bias current between the body region and the source region.

44. (**Previously Presented**): The memory cell of claim 43 wherein the second charge is stored in the body region in response to removing the first positive voltage from the drain region and the second positive voltage from the gate.

45. (**Previously Presented**): The memory cell of claim 37 wherein the first charge is stored in the body region in response to applying a first negative voltage to the drain region and a second negative voltage to the gate.

46. (**Previously Presented**): The memory cell of claim 45 wherein the transistor of the memory cell stores the first charge in a portion of the body region that is adjacent to the source region.

47. (**Currently Amended**): A semiconductor memory cell including at least one transistor to constitute the memory cell, the at least one transistor of the memory cell comprising:

a source region having impurities to provide a first conductivity type;

a drain region having impurities to provide the first conductivity type;

a body region disposed between the source region and the drain region wherein the body region is electrically floating and includes impurities to provide a second conductivity type wherein the second conductivity type is different from the first conductivity type;

a gate spaced apart from, and capacitively coupled to, the body region;

wherein the memory cell includes:

a first data state representative of a first charge in the body region; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region.

48. **(Previously Presented)**: The memory cell of claim 47 wherein, in response to a first voltage applied to the drain region and a second voltage applied to the gate, the first charge is removed from the body region through the source region.

49. **(Previously Presented)**: The memory cell of claim 48 wherein, in response to removing the first voltage from the drain region before removing the second voltage from the gate, the second charge is stored in the body region.

50. **(Previously Presented)**: The memory cell of claim 48 wherein the second charge is stored in the body region in response to applying ground to the drain region before removing the second voltage from the gate.

51. **(Previously Presented)**: The memory cell of claim 48 wherein the first voltage and the second voltage are positive voltages which, during operation, are applied for a finite duration.

52. **(Previously Presented)**: The memory cell of claim 48 wherein the transistor, in response to the first voltage and the second voltage, includes a junction between the body region and the source region which is forwarded biased.

53. **(Previously Presented)**: The memory cell of claim 52 wherein the first voltage and the second voltage are positive voltages which are applied for a finite duration.

54. **(Previously Presented)**: The memory cell of claim 53 wherein, in response to the positive voltages being applied to the drain region and the gate, the transistor includes a forward bias current between the body region and the source region.

55. **(Previously Presented)**: The memory cell of claim 54 wherein the transistor stores the second charge in the body region in response to a third voltage being applied to the drain region before a fourth voltage is applied to the gate.

56. **(Previously Presented)**: The memory cell of claim 55 wherein the third and fourth voltages are ground.

57. **(Previously Presented)**: The memory cell of claim 48 wherein the transistor stores the first charge in a portion of the body region that is adjacent to the source region.

58. **(Previously Presented)**: The memory cell of claim 57 wherein the first charge is substantially provided by impact ionization.

59. (**Previously Presented**): The memory cell of claim 48 wherein, in response to a first positive voltage applied to the drain region and a second positive voltage applied to the gate, more than the first charge is removed from the body region through the source region.

60. (**Previously Presented**): The memory cell of claim 59 wherein the first positive voltage is less than the second positive voltage.